

Patent Claims:

1. An analysis device for an embedded system (9) comprising a CPU (1), a CPU bus (2), and a memory (3), and including at least one communication module (4) for the input or output of analysis data by way of a test interface (5),
c h a r a c t e r I z e d in that the communication module permits the internal memory and input and output access operations of the embedded system to be monitored and/or logged without using the clock cycles of the CPU (1).
2. The analysis device as claimed in claim 1,
c h a r a c t e r i z e d by two, in particular at least three freely selectable analysis modes, with the analysis modes, in the way and extent of participation of the CPU 1, differing from each other in the read and/or write operations of data for analyzing purposes.
3. The analysis device as claimed in claim 2,
c h a r a c t e r i z e d in that depending on the selected analysis mode, either
 - all write access operations of the CPU are logged to especially definable address ranges without using clock cycles, or
 - all read access operations of the CPU are logged, or
 - direct reading and writing of the CPU out of/into an external memory (6) is executed by using clock cycles.
4. The analysis device as claimed in at least one of claims 1 to 3,

c h a r a c t e r i z e d in that the communication module comprises a controller which, by way of a connection to the data bus and/or the control bus and/or the address bus, can independently make access to this bus/these buses of the embedded system in order to monitor write and/or read access operations in real time, that means without influencing of the CPU.

5. The analysis device as claimed in at least one of claims 1 to 4,

c h a r a c t e r i z e d in that the communication module is connected to a buffer store (8) or in particular comprises said, and the data transferred in write and/or read access operations can be stored in the buffer store.

6. The analysis device as claimed in at least one of claims 1 to 5,

c h a r a c t e r i z e d in that data can be output from the buffer store in a buffered fashion by way of test interface (5) or data can be read into the buffer store by way of this interface.

7. The analysis device as claimed in at least one of claims 1 to 6,

c h a r a c t e r i z e d in that the external test code memory (6) is a magnetic core memory or a dual-port memory.

8. The analysis device as claimed in at least one of claims 1 to 7,

- c h a r a c t e r i z e d in that the communication module (4) is integrated into the embedded system.
9. The analysis device as claimed in at least one of claims 1 to 8,
c h a r a c t e r i z e d in that the test interface (5) is connected to a test code memory (6) arranged outside the embedded system.
10. The analysis device as claimed in at least one of claims 1 to 9,
c h a r a c t e r i z e d in that the data transfer from the communication module to the external memory takes place by way of a parallel interface.
11. The analysis device as claimed in at least one of claims 1 to 10,
c h a r a c t e r i z e d in that the external memory (6) is connected to a data conditioning device (7) providing an interface connection (14) to external debugging applications.
12. An embedded system comprising a central processor unit (1), a CPU bus (2) and a memory (3),
c h a r a c t e r i z e d in that the system comprises an analysis device as claimed in at least one of claims 1 to 11.
13. A method for the analysis of an embedded system with an analysis device as claimed in at least one of claims 1 to 11,
c h a r a c t e r i z e d in that at least one mode is provided in which the analysis data in real time can be read out of the system that comprises at least CPU, data memory,

program memory and input/output element(s), and/or can be written in the system so that the system need not be stopped or interrupted, respectively, for the analysis.

14. The method as claimed in claim 13,
c h a r a c t e r i z e d in that

- the memory content or a correspondingly assessable information of the embedded system, in whole or in part, is copied in real time into an external memory, with the data being buffered in particular before this operation, and/or
- the data content of an external memory (6) or a correspondingly assessable information about the memory content of the memory (6), in whole or in part, is copied in real time into a memory of the embedded system, with the data being buffered in particular before this operation.

15. The method as claimed in claim 13 or 14,
c h a r a c t e r i z e d in that the external memory is used to transmit data for typical debugging applications.

16. The method as claimed in at least any one of claims 13 to 15,
c h a r a c t e r i z e d in that only the data needed for debugging is transferred to the external memory (6) in the event of access operations of the CPU to RAM 3.

17. The method as claimed in at least any one of claims 13 to 16,

c h a r a c t e r i z e d in that write access operations and/or read access operations of the CPU are logged by means of a buffer store.

18. The method as claimed in claims 13 to 17,
c h a r a c t e r i z e d in that information about the write access operations is written without additional CPU commands into the buffer store (8) or directly into the communication module (4), and the information about the read access operations is written into the buffer store with active assistance of the CPU.
19. The method as claimed in at least any one of claims 13 to 18,
c h a r a c t e r i z e d in that a mode of the embedded system is provided in which all write and/or read access operations of the CPU are rerouted to the communication module.
20. The method as claimed in at least any one of claims 13 to 19,
c h a r a c t e r i z e d in that a mode of the embedded system is provided in which only either the write access operations or the read access operations of the CPU are rerouted to the communication module, and the other access operations of the CPU to the memory are logged actively by the CPU into the external memory.